**Remarks/Arguments**

**Status of the Application**

Applicant respectfully requests reconsideration of the rejections and objections set forth in the Office Action mailed on September, 20, 2006.

The Examiner has rejected claims 38, 42, 47, and 50 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,896,380 to *Brown et al. (Brown)* in view of U.S. Patent No. 6,324,165 to *Fan et al. (Fan)*.

The Examiner has further rejected claims 39, 40, 44, and 45 under 35 U.S.C. 103(a) as being unpatentable over *Brown* in view of *Fan*, and further in view of U.S. Patent No. 6,751,219 to *Lipp et al. (Lipp)*.

The Examiner has further rejected claim 43 under 35 U.S.C. 103(a) as being unpatentable over *Brown* in view of *Fan*, and further in view of U.S. Patent No. 6,473,428 to *Nichols et al. (Nichols)*.

The Examiner has further rejected claims 48-49 under 35 U.S.C. 103(a) as being unpatentable over *Brown* in view of *Fan*, and further in view of U.S. Patent No. 6,661,773 to *Pelissier et al. (Pelissier)*.

The Examiner has further rejected claims 41 and 46 under 35 U.S.C. 103(a) as being unpatentable over *Brown* in view of *Fan*, and further in view of U.S. Patent No. 6,122,279 to *Milway et al. (Milway)*.

As such, claims 38-50 are pending in this application.

**The Claims**

**Cited Art**

*Brown*

*Brown* describes a multi-stage ATM switch having "a plurality of inlet stage fabrics, core stage fabrics, and outlet state fabrics," (Abstract). Brown describes methods of creating loading a core stage fabric with data cells and added cells to preserve length and rank between cells (*see* FIG. 3; Col. 6, ll. 27-41). By ordering cells in the core stage fabric, cells from a burst are all aligned (*see* Col. 6, ll. 40-41).

*Fan*

*Fan* describes large capacity ATM core switch architectures which utilize scheduling techniques based on observed bottleneck points within the switch (*see* Abstract).

*Lipp*

*Lipp* discloses methods for performing multicasts in a packet-based network (*see* Abstract).

*Nichols*

*Nichols* discloses a multi-stage switch that utilizes internal logic for preserving temporal order of the cells (*see* Abstract).

*Pelissier*

*Pelissier* discloses methods for detecting and discarding stale cells following a route change in a data communication network (*see* Abstract).

*Milway*

*Milway* discloses methods for switching ATM cells from inputs to outputs utilizing a token bus allocation scheme (*see* Abstract).

**Rejections Under 35 U.S.C. § 103 (a)**

Claims 38, 42, 47, and 50

The Examiner has rejected claims 38, 42, 47, and 50 under 35 U.S.C. 103(a) as being unpatentable over *Brown* in view of *Fan*. Applicant respectfully traverses.

As noted above, *Brown* describes a multi-stage ATM switch having "a plurality of inlet stage fabrics, core stage fabrics, and outlet state fabrics," (Abstract). *Brown* describes methods of creating loading a core stage fabric, which the Examiner has compared with the "intermediate layer of claim 37, with data cells and added cells to preserve length and rank between cells (*see* FIG. 3; Col. 6, ll. 27-41). By ordering cells in the core stage fabric, cells from a burst are all aligned (*see* Col. 6, ll. 40-41). Indeed, *Brown* clearly discloses the functioning aspects of the queue,

> When the queuer 66 of core stage fabric 20-1 receives cell "A", it examines sub-field 44 (FIG. 2) of its destination field 42 (FIG. 2) and, based on this examination, places the cell in a queue 64, in this case queue 64-3 representing the third outlet stage fabric 24-3. The queuers of core stages 20-II 20-III and 20-IV similarly act to place each of cells "B", "C", and "D" in their queues representing outlet stage fabric 24-3... If, per chance, scheduler 58 of inlet stage fabric 14-1 finds no queue with four cells to transmit, it may choose the queue with the greatest number of cells and pad this queue up to four cells with "blank" ATM cells (i.e. cells with no payload data) so that the scheduler may transmit cells when requested. (col. 5, l. 62 – col. 6, l. 14; emphasis added).

In contrast, the present claims require no such elements. Indeed, as noted by the Specification at paragraph 0043, "Each intermediate layer circuit delivers cells to the output layer 103 as the cells arrive." Thus, comparison of *Brown's* method of queuing at a core stage fabric (intermediate layer) is inapposite with respect to the present claims since the present claims anticipate no such queuing. Still further, claim 38, as amended, requires a buffer, "wherein the buffer is configured to release the selected cell on a continuous basis." Applicant submits that no new matter has been added. Support for the proposed amendment may be found in the Specification at ¶ 0030.

In addition, claim 42 requires that the intermediate layer sends, "said selected cell as said selected cell arrives at said selected intermediate layer circuit." Thus, methods provided herein each require a buffer, which is not disclosed by *Brown*.

Therefore, for at least these reasons, Applicant submits that *Brown* does not reasonably suggest or described as required by claims 38 and 42.

In addition, as noted above, *Fan* describes large capacity ATM core switch architectures which utilize scheduling techniques based on observed bottleneck points within the switch (*see* Abstract). *Fan*, however, does not disclose an intermediate layer that utilizes a buffer which immediately forwards packets to an output layer. Therefore, Applicant submits that *Fan* does nothing to reasonably suggest or cure the deficiency in *Brown*.

All remaining claims depend directly from independent claim 42 and are therefore patentable over the cited art for at least the same reasons cited for claim. Therefore, for at least

these reasons, Applicant respectfully submits that the present claims are allowable over the cited art and requests that the above rejection be removed.

Claims 39, 40, 44, and 45

The Examiner has further rejected claims 39, 40, 44, and 45 under 35 U.S.C. 103(a) as being unpatentable over *Brown* in view of *Fan*, and further in view of *Lipp*. Applicant respectfully traverses.

As an initial matter, claims 39, 40, 44, and 45 depend either directly or indirectly from independent claims 38 and 42 and are therefore allowable over the cited art for at least the same reasons cited for claims 38 and 42. Furthermore, *Lipp* discloses methods for performing multicasts in a packet-based network (*see* Abstract), but does nothing to suggest or cure the deficiency in *Brown*.

Therefore, for at least these reasons, Applicant respectfully submits that the present claims are allowable over the cited art and requests that the above rejection be removed.

Claim 43

The Examiner has further rejected claim 43 under 35 U.S.C. 103(a) as being unpatentable over *Brown* in view of *Fan*, and further in view of *Nichols*. Applicant respectfully traverses.

As an initial matter, claim 43 depends directly from independent claim 42 and is therefore allowable over the cited art for at least the same reasons cited for claim 42. Furthermore, *Nichols* discloses a multi-stage switch that utilizes internal logic for preserving temporal order of the cells (*see* Abstract), but does nothing to suggest or cure the deficiency in *Brown*. Still further, *Nichols* discloses a multi-stage switch which utilizes markers to indicate transmissions of cells (*see* col. 5, ll. 24-38), which is not related to cell volume as required by the present claims.

Therefore, for at least these reasons, Applicant respectfully submits that the present claim is allowable over the cited art and requests that the above rejection be removed.

Claims 48-49

The Examiner has further rejected claims 48-49 under 35 U.S.C. 103(a) as being unpatentable over *Brown* in view of *Fan*, and further in view of *Pelissier*. Applicant respectfully traverses.

As an initial matter, claims 48-49 depends directly from independent claim 42 and are therefore allowable over the cited art for at least the same reasons cited for claim 42. *Pelissier* discloses methods for detecting and discarding stale cells following a route change in a data communication network (*see* Abstract), but does nothing to suggest or cure the deficiency in *Brown*. Still further, *Pelissier* discloses methods whereby a blocked switch may be bypassed utilizing redundant paths (*see* col. 4, ll. 4-54), which is not related to layer circuitry as required by the present claims.

Therefore, for at least these reasons, Applicant respectfully submits that the present claims are allowable over the cited art and requests that the above rejection be removed.

Claims 41 and 46

The Examiner has further rejected claims 41 and 46 under 35 U.S.C. 103(a) as being unpatentable over *Brown* in view of *Fan*, and further in view of *Milway*. Applicant respectfully traverses.

As an initial matter, claims 41 and 46 depend directly from independent claims 38 and 42 and are therefore allowable over the cited art for at least the same reasons cited for claims 38 and 42. Furthermore, *Milway* discloses methods for switching ATM cells from inputs to outputs utilizing a token bus allocation scheme (*see* Abstract), but does nothing to suggest or cure the deficiency in *Brown*. Still further, *Milway* discloses ports each having two transmit FIFOs or queues (*see* col. 17, ll. 34-37), which is not related to a high priority traffic intermediate layer circuit as required by the present claims.

Therefore, for at least these reasons, Applicant respectfully submits that the present claims are allowable over the cited art and requests that the above rejection be removed.

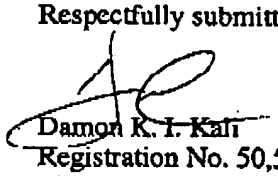
**Conclusion**

In view of the above remarks, reconsideration and allowance of the claims are respectfully requested entry under 37 CFR § 1.116. Should the Examiner believe that a

telephone conference would expedite the prosecution of this application; the undersigned can be reached at the telephone number set out below.

The Commissioner is authorized to charge any additional fees to process this Amendment, or credit any over-payments that may apply, to our Deposit Account No. 50-2421 (Order No. RAZA-01001).

Respectfully submitted,



Damon K. I. Kali
Registration No. 50,541

Tel: 408-288-5068